

FE Electronics Planning

K. Einsweiler, LBNL

Discuss next steps with FE-D2 and TEMIC

- Expected “wafers out” date from TEMIC is Oct. 16 (week 42), one week later than originally foreseen. Still waiting for detailed confirmation.
- Many things to synchronize (testing of all parts, possible irradiations, etc.)

Situation with Honeywell SOI

- New cost information received, indicating cost increase of factor roughly 2.5, making this process un-affordable for ATLAS pixels.

Combination of yield and technology problems with DMILL and cost increases from Honeywell makes it imperative to begin working in 0.25 μ technologies:

- There was a 3-day FE workshop in LBL Sept 20-22, where a first discussion of the goals, tasks, and schedules took place.
- There was a more comprehensive workshop at CERN last week (Sept. 27).

FE-D2 and TEMIC Planning

Two runs in progress with TEMIC:

- Standard 8-wafer engineering run with FE-D2 devices (FE-D2S and FE-D2D, MCC-D2, VDC-P2, DORIC-P2, plus miscellaneous test chips and test structures).
- Experimental 22-wafer run with same reticle, but with corners for three critical variations agreed to by LETI and TEMIC, with the hope of determining the source of the technology problems which caused extremely low yields on FE-D1 chips.
- Wafers will be divided into two identical groups, and shipped directly to Bonn and LBL for testing. LBL plans to rapidly test FE chips on one wafer, have it diced, and then distribute parts (package 10-25 MCC-D2, distribute bare die for PM-bars, Analog Test Chips, VDC-P2, DORIC-P2, etc.) to design groups for very quick evaluation.

Critical to evaluate this run rapidly:

- For FE chips, goal is first evaluation for Dec pixel week, to decide how to proceed with TEMIC, and how to divide resources between TEMIC and 0.25 μ work.
- For MCC-D2, need to understand whether TEMIC is a real vendor, and if not, begin rapid conversion to 0.25 μ .
- For VDC/DORIC, indications are that TEMIC could be a vendor, but need to make sure that DORIC works well.

Evaluation steps for FE-D2 Run

FE-D2 evaluation:

- First, study results at wafer probe level in Bonn and LBL. Understand differences between behavior and yield for FE-D2D and FE-D2S.
- If either version of the FE-D2 looks like it operates reasonably well, send wafers for bump-bonding, and also prepare test boards for PS irradiation.
- As soon as “experimental” wafers are available, carry out yield and test measurements for them, and look for “smoking guns” pointing to origin of low FE-D1 yield. Possibly buy some wafers from experimental run for bumping, etc.

MCC-D2 evaluation:

- Genova will already be irradiating MCC-D0 in PS beam in Oct, using newly designed test system for this purpose.
- Will prepare packaged MCC-D2 for Genova as rapidly as possible. Genova will study yield and performance, and decide whether they are worth irradiating in PS this year.

DORIC-P2/VDC-P2 evaluation:

- Dice parts as rapidly as possible and send to Siegen/OSU/Wuppertal for evaluation.
- If they work well, try to irradiate in PS as well ? Lower priority than above...

Test Chips:

- Previous results with Analog Test chips indicated failure after moderate doses, inconsistent with results from single transistors in PM bars. These need to be repeated if possible with the new test chips.
- Previous results with PM bars showed large shifts, but no fundamental problems. These irradiations were performed un-biassed. It would be useful, but not essential, to irradiate more bars with “worst-case” bias (NMOS turned on, PMOS turned off).

Comments:

- Given the very late delivery of the wafers from TEMIC (and they are not delivered yet !), it is extremely difficult to test and prepare parts for testing in the PS run.
- The PS run continues to Nov 13, but we would need to have any new assemblies by approximately Nov 1 in order to be able to expose them to significant doses (one week required to expose device to full pixel fluence). Also, there are presently only 8 slots available in the cold box and so competition for space may be fierce.
- We will do our best to get this ready, but a large coordinated effort from many people will be needed !
- In addition, we are preparing setup to do irradiations at LBL in Dec or later. However, only one board at a time (55 MeV), so not “production” like PS.

Proceeding towards 0.25 μ versions of Pixel Chips

Background:

- We now have at most one vendor for our rad-hard designs in pixels.
- We have found that our designs must be more aggressive to fit within the restrictions imposed by DMILL (dynamic logic, little SEU tolerance, operation over very large parameter variations, very large die size, etc.). This requires extra engineering and testing, and there is extra risk.
- This makes it imperative to develop 0.25 μ versions of our pixel chips (FE, MCC, VDC, DORIC), or we risk having nothing with which to construct ATLAS.

Topics and Goals for LBL FE-I Workshop:

- Discuss special concerns for using 0.25 μ processes - remaining risks ?
- Discuss current FE-H and FE-D designs, and evaluate block by block what changes are necessary or desirable. First agreements on who will do what.
- Discuss technology issues (TSMC vs IBM rules, metal layers, linear caps, etc.)
- Discuss design methods (top-down design, synthesis, CAD tools) and upgrades to design kit (back-annotated Verilog, SEU-tolerant cells, substrate contacts, etc.)
- Do we prototype in TSMC/IBM MPW first or go directly to engineering run ?
- Everyone agreed to proceed as rapidly as possible...

Major Issues for FE-I Conversion:

- Basic idea is to develop conservative chip, like FE-H, based on 400μ pixel, about 32 EOC buffers, and overall with the same basic design.
- Need significant changes in present front-end design for feedback and threshold control, which rely on small W/L NMOS devices which cannot be built in 0.25μ with annular layouts.
- Have significant concerns about SEU tolerance of designs, and several solutions are available for this (error correcting registers, more robust state machine designs, etc.)
- For digital readout, propose to move towards a fully static readout design, to minimize impact of SEU and leakage.
- Also a new idea to include digital timewalk correction in CEU based on TOT values. This could give us more flexibility in achieving timewalk specs, which have proved marginal and difficult to improve in our present complete chips.

Held ATLAS Pixel 0.25μ Workshop on Sept 27:

- General discussion of RD-49 results and pixel issues with Walter Snoeys.
- Discussion of conversion issues for each of pixel chips (FE, MCC, VDC, DORIC).
- Discussion of involvement of additional manpower from NIKHEF, Milano, UOK.

Conclusions:

- Agreement to proceed on FE-I as rapidly as possible.
- Major issue is how best to create new front-end design. Can either proceed via rapid MPW prototype, followed by engineering run (early delivery of design, but with measurements before full run) or via careful, well-simulated design with no prototype measurements. This requires further study.
- Constraints placed by need to fully characterize and qualify a new design with a new vendor during 2001 suggest an engineering run is required by Jun 1 2001.
- Discussed conversion issues for MCC-D2. Since the design is driven by high-level (Verilog) description, with limited use of full-custom blocks, conversion should be relatively easy. Given needs for continued evaluation of MCC-D0 and MCC-D2 on rapid schedule, would expect to begin real work on this in Jan 2001, with goal of submitting a complete prototype when FE-I is ready.
- Discussed conversion issues for VDC and DORIC. Present groups are eager to begin investigating conversion, and would expect to produce new designs either for an MPW run in early 2001, or for the FE-I engineering run.
- There is potentially a large conflict between resources needed for the work above, and resources needed to develop pre-production quality DMILL versions of the chips in the FE-D2 run. We will re-discuss all of these issues in Dec pixel week, based on first results from characterizing chips from FE-D2 run.